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Description

The present invention concerns digital electronic circuits and more particularly it relates to an automatic system for adjusting the output impedance of fast CMOS drivers.

It is known that when a driver is to send a digital flow to a far receiver through a transmission line can present some problems in the case in which there is no good matching between transmission line impedance and input and output impedances of the circuits connected therewith. Generally, in these cases there are power losses and multiple reflections which can cause an error probability increase in the symbol reception since at a certain instant, beside the symbol transmitted in the present time interval, there are at the receiver the symbols transmitted in the preceding time intervals reflected by the line ends.

Said disadvantages can be eliminated if at least the driver output impedance is rendered equal to the characteristic impedance of the line: in fact, even though there is a mismatch at the output connected to the receiver, the input impedance of a rather long line is almost equal to the characteristic line impedance, that would entail a reflection at the far end of the line, but the reflected signal is absorbed at the input by the driver output impedance, whose value is equal to the line impedance, thus avoiding multiple reflections.

Under these conditions the receiver receives only the direct signal, whose amplitude is twice as wide as an effect of overlapping between the direct signal and the signal immediately reflected, of course under the hypothesis that the receiver input impedance exceeds characteristic line impedance.

However, drivers with output impedance equal to the the characteristic impedance of the usual transmission lines are not easy to build, owing to unavoidable variations due to fabricating process tolerances. Besides, the same transmission lines can present tolerances in the characteristic impedance. It is hence advisable to think of an automatic system for adjusting the driver output impedance so as to obtain a good matching to the line, independant of fabrication tolerances and accidental circuit variations.

It is also convenient that the driver output impedance be made equal to the characteristic line impedance without using an external additional resistance, in order to avoid an oversizing of the output circuit with consequent speed loss and power consumption.

A solution to said problems has been described in the article entitled "A Self-Terminating Low-Voltage Swing CMOS Output Driver" by Thomas F.Knight et alii, issued in IEEE Journal of Solid State Circuits, Vol.23, No.2, April 1988.

According to this solution, the output impedance of a plurality of drivers contained in the same integrated circuit is controlled by a suitable circuit, still housed in the same integrated circuit, comprising a driver, analogous to those controlled, and a receiver. The control driver sends a clock signal, locally-generated to a unique control aim, on a transmission line length with the same characteristics as those of the lines connected to controlled-driver outputs. The line output is connected to the receiver input, that extracts from the received signal an enabling signal synchronized to logic-level transitions.

The voltage at the input of the reference line is read continuously by a threshold comparator, whereby it is compared with a threshold voltage of value equal to half the maximum value of the output voltage of the driver under matching conditions.

The information at the output of the comparator is considered valid, and can be used for control aims, only at the instant when the receiver has detected a transition on the line after a delay slightly exceeding reference line propagating time, permitting the line voltage to stabilize at a level dependant on reflection coefficient value at the transmission end.

It is clear that in case of impedance matching between the driving line and the reference line the voltage at the line input, upon transmission of an edge, is equal to half the maximum value of the output voltage at the transmission end, that is why in this case the comparator does not supply any output signal. On the contrary, if there is no matching, the information relevant to the algebraic difference with respect to threshold is used to vary a pulsed voltage across the terminals of a high-value capacitor, which is placed outside the integrated circuit. Therefore, the amplitude of this voltage varies in function of the reflection coefficient at the reference line input.

A CMOS driver output impedance can be controlled by varying the gate voltage of the two transistors of the output stage, within certain limits determined by the geometrical dimensions of the transistors themselves. To obtain this control, the predriver stages have to be fed with a suitable voltage, which, in case of the solution described in the cited article is the pulsed voltage present at the external-capacity terminals. This voltage, besides matching the reference driver output impedance to the reference line, matches also the output impedance of all the other slaved drivers, being utilized to feed also all the other predriver stages.

If line voltage exceeds threshold voltage at the comparator input, the capacitor is continuously discharged by a proper non-negligible power circuit, owing to considerable external capacity value, whilst in the opposite case the capacitor is charged and supplies current to all the predriver stages at the transition, up to the obtention of an optimal value corresponding to impedance matching condition.

However this circuit presents a number of disadvantages. A first disadvantage is due to the fact that during the initial adjusting phase at both line ends there is impedance mismatch, and hence there is a multiple reflection condition. As a consequence when a reflected edge goes back to the emitter to alter the line voltage level in the time interval in which the information is taken as valid, an error can be generated which sets the circuit in an adjustment condition difficult to envisage.

Another disadvantage is due to threshold comparator response time, which must be much lower than the delay introduced by the reference transmission line, since when the receiver has detected the level transition for generating the signal enabling the reading of line voltage, the comparator output must be at the steady-state value. This delay, dependant on line length, is usually very small (of the order of ns) since the line is short. Besides if a low error is desired, the differential voltage at the comparator inputs must very low and that implies a very sophisticated comparator.

Finally this circuit needs a big capacitor, which is not integrable and hence is to be placed ouside. Also the driving of this capacitor needs power circuits, with consequent speed loss.

Said disadvantages are overcome by the automatic system for adjusting the output impedance of fast CMOS drivers, provided by the present invention, which does not present multiple reflection condition during the initial output impedance adjusting, does not require a high performance threshold comparator, neither requires a big capacitor difficult to integrate and avoids mutual interference among slaved drivers.

The present invention provides an automatic system for adjusting the output impedance of fast CMOS drivers, wherein the output impedance of a plurality of slaved drivers is controlled by a circuit for measuring and correcting mismatch between one of the drivers, taken as reference and dedicated to this aim, and the impedance at the input of a reference transmission line, equal to lines connected to the other drivers, the output impedance adjustment of the reference driver being carried out by a comparator comparing the maximum voltage of a clock signal supplied by that reference driver at the input of the reference line with a reference voltage equal to half the supply voltage of the output stage of the drivers and dependant on the result of the comparison said comparator supplies a current which periodically charges or discharges a capacitor, so as to obtain across its terminals a control voltage for the driver impedance, characterized in that a first clock signal is sent to the input of said reference driver producing a periodic signal on said reference line terminated by a resistance equal to its characteristic impedance and said periodic signal present at the reference line input is compared with said reference voltage in a threshold comparator in correspondance with the transitions of a second clock signal with a frequency equal to that of the first clock signal, but in quadrature so as to carry out the comparison at the center of the half-period wherein the voltage at the input of the reference line is maximum, the comparison result being used to charge or discharge a capacitor, whose voltage is applied to the input of a plurality of buffer amplifiers, one of which controls the output impedance of the reference driver and the others the output impedance of the slaved drivers.

The foregoing and other characteristics of the present invention will be made clearer by the following description of a preferred embodiment thereof, given by way of non-limiting example, and by the annexed drawing representing the electrical circuit diagram of the automatic system.

According to the invention, a circuit for the measurement and correction of mismatch between the output impedance of a reference driver DM, dedicated to this aim, and the characteristic impedance of a transmission line L, equal to lines L1...Ln connected to the other drivers, terminated by a resistance R equal to this characteristic impedance, is added in an integrated circuit comprising a plurality of drivers DS1...DSn.

The output impedance of reference driver DM is measured by measuring the input voltage of line L, which under perfect matching conditions is equal to half the supply voltage of the output stage of the driver, consisting of transistors MA and MB. Said transistors are fed at a terminal 1 with a well-determined and constant voltage, whose value is equal to 1V, owing to high transmission rate demanded of such drivers, e.g. 160 Mbit/s. As a consequence, under perfect matching conditions, at the input of transmission line L maximum signal amplitude is 0.5V, whilst under mismatch conditions this value changes and the system operates so as to vary the output impedance of the reference driver DM till a maximum voltage of 0.5V is reached again.

The reference driver receives at its inputs 2 and 3 a clock signal and its complementary signal, generated by a suitable generator not shown in the Figure. These signals present a frequency inferior to data bitrate at inputs 21, 31..2n, 3n of the other slaved drivers DS1 ...DSn, but equal edge steepness in order to maintain the same behaviour in presence of transitions. It is thus possible to uniform the step response of reference line L to that of the other lines L1 ...Ln, connected to corresponding receivers RX1,...,RXn. More particularly, clock signal frequency can be equal to about one fourth of transmitted signal bit rate.

The circuit for measuring and correcting impedance mismatch consists of a threshold comparator CO, which compares 0.5 V reference voltage, applied to the terminal 4 of level translating circuit LS1, with the voltage measured at line L input and equally level translated by a translating circuit LS2, receiving it via wire 5. Said translating circuits LS1 and LS2 are render d n necessary to meet common-mode dynamic-range requirements of threshold comparator CO.

The comparison is carried out by threshold comparator CO under the control of a clock signal applied to input 6. This signal has the same characteristics as the signal applied to input 2 of the driver DM, but it leads this latter by a 90° phase so as to guarantee that the voltage reading at the input of transmission line L takes always place in correspondence with the high voltage level.

The automatic system for impedance matching operates as follows. When the clock signal at input 6 is at low level, the signals at both outputs connected to wires 7 and 8 are at high level and hence P-MOS transistors MC and MD are cut off. As a consequence no charge is supplied to capacitor C1, which keeps unchanged the voltage across its terminals.

When the clock signal at input 6 undergoes a transition from low level to high level, threshold comparator CO effects the comparison between the voltage at the the input of reference line and the reference voltage at input 4.

If the line voltage is higher than the reference voltage, the only signal on wire 7 passes to low level, turning on transistor MC, which supplies a certain quantity of electrical charge to capacitor C1, increasing the voltage across its terminals. A buffer amplifier BU, whose input is connected to capacitor C1, supplies a supply voltage variation, opposite to voltage variation on C1, to two inverters I1 and I2 on wire 9. Said inverters drive in turn transistors MA and MB, placed at reference driver output, with a voltage controlling the differential output resistance of transistor MA increasing its value and thus reducing the voltage present at the input of reference line L. More particularly, under these conditions a voltage equal to that present on wire 9, is rendered available to all slaved drivers DS1...DSn by the same number of buffer amplifiers BU1...BUn, whose inputs are connected to capacitor C1. Thus decoupling is carried out between the different drivers and at the same time the high current demanded during switching phase, owing to higher operation speed, is supplied to inverters I11, I21..., which drive transistors MA1, MB1... of the other slaved drivers.

Of course if line voltage is lower than reference voltage, the circuit operation takes place so as to produce an opposite effect to that just examined on the output resistance of reference driver DM.

More particularly if line voltage is lower than the reference voltage, the only signal on wire 8 passes to low level, turning on transistor MD, which substracts a certain charge quantity from capacitor C1, reducing the voltage across its terminals. Buffer amplifier BU supplies a variation in supply voltage opposite to voltage variation on C1 to the two inverters I1 and I2, driving transistors MA and MB with a voltage controlling the output differential resistance of transistor MA by reducing its value and hence increasing the voltage present at the input of reference line L.

It is worth noting that voltage outgoing from comparator CO is maintained constant for the whole clock signal period on wire 6 and that the comparison takes place after both outputs 7 and 8 pass to high logic level. In this way the electrical charge quantity transferred to capacitor C1 is only proportional to the half-period of the clock signal on wire 6.

It is clear that what described has been given only by way of an example. Variations and modifications are possible.

Claims

1. An automatic system for adjusting the output impedance of fast CMOS drivers, wherein the output impedance of a plurality of slaved drivers (DS1...DSn) is controlled by a circuit for measuring and correcting mismatch between one of the drivers (DM), taken as reference and dedicated to this aim, and the impedance at the input of a reference trans-mission line (L), equal to lines (L1...Ln) connected to the other drivers, the output impedance adjustment of the reference driver (DM) being carried out by a comparator (CO) comparing the maximum voltage of a clock signal supplied by that reference driver (DM) at the input of the reference line (L) with a reference voltage equal to half the supply voltage of the output stages of the drivers and dependant on the result of the comparison said comparator (CO) supplies a current which periodically charges or discharges a capacitor (C1), so as to obtain across its terminals a control voltage for the driver impedance, characterized in that a first clock signal is sent to the input (2, 3) of said reference driver (DM) producing a periodic signal on said reference line (L) terminated by a resistance (R) equal to its characteristic impedance and said periodic signal present at the reference line input is compared with said reference voltage in said comparator (CO) in correspondence with the transitions of a second clock signal (on 6) with a frequency equal to that of the first clock signal, but in quadrature so as to carry out the comparison at the center of the half-period wherein the voltage at the input of the reference line (L) is maximum, the comparison result being used to charge or discharge the capacitor (C1), whose voltage is applied to the inputs of a plurality of buffer amplifiers, one (BU) of which controls the output impedance of the reference driver (DM) and the others (BU1...BUn) the output impedances of the slaved drivers (DS1...DSn).

2. An automatic system as in claim 1, characterized

in that said clock signals present a frequency lower than the bit rate of data at the inputs of the slaved drivers (DS1...DSn), but an equal edge steepness.

3. An automatic system as in claim 1 or 2, characterized in that said clock signals present a frequency equal to about a fourth of the bitrate of the data at the inputs of the slaved drivers (DS1...DSn).

4. An automatic system as in any of claims 1 to 3, characterized in that the output voltage from said comparator (CO) is constant for the whole period of the second clock signal and that the comparison takes place after its outputs (7, 8) pass to high logic level.

Patentansprüche

1. Automatisches System zum Justieren der Ausgangsimpedanz schneller CMOS-Treiber, bei dem die Ausgangsimpedanz einer Vielzahl abhängiger Treiber (DS1, ..., DSn) durch eine Schaltung zum Messen und Korrigieren einer Fehlanpassung zwischen einem der Treiber (DM), der als Referenz verwendet und zu diesem Zweck bestimmt ist, und der Impedanz am Eingang einer Referenz-Übertragungsleitung (L) gleich den mit den anderen Treibern verbundenen Leitungen (L1, ..., Ln) gesteuert wird und die Ausgangsimpedanzjustierung des Referenztreibers (DM) von einem Komparator (CO) durchgeführt wird, der die Maximalspannung eines Taktsignals, das vom Referenztreiber (DM) am Eingang der Referenzleitung (L) geliefert wird, mit einer Referenzspannung gleich der halben Speisespannung der Ausgangsstufe der Treiber vergleicht, und der Komparator (CO) in Abhängigkeit vom Vergleichsergebnis einen Strom liefert, der periodisch einen Kondensator (C1) lädt oder entlädt, wodurch an den Kondensatorklemmen eine Steuerspannung für die Treiberimpedanz zu erhalten ist, dadurch gekennzeichnet, daß ein erstes Taktsignal an den Eingang (2, 3) des Referenztreibers (DM) angelegt ist, der ein periodisches Signal auf der Referenzleitung (L), die von einem Widerstand (R) mit einem Widerstandswert gleich der charakteristischen Impedanz abgeschlossen ist, erzeugt, und daß das am Eingang der Referenzleitung liegende periodische Signal mit der Referenzspannung im Komparator (CO) verglichen wird, und zwar in Übereinstimmung mit den Übergängen eines zweiten Taktsignals (auf 6) mit einer Frequenz gleich der des ersten Taktsignals, jedoch in Quadratur so, daß der Vergleich in der Mitte der Halbperiode stattfindet, in der die Spannung am Eingang der Referenzleitung (L) Maximum ist, und daß das Vergleichsergebnis dazu dient, den Kondensator (C1) zu laden oder zu entladen, dessen Spannung an den Eingang einer Vielzahl von Pufferverstärkern angelegt ist, von denen einer (BU) die Ausgangsimpedanz des Referenztreibers (DM) steuert und die anderen (BU1, ..., BUn) die Ausgangsimpedanz der abhängigen Treiber (DS1, ..., DSn) steuern.

2. Automatisches System nach Anspruch 1, dadurch gekennzeichnet, daß die Taktsignale eine Frequenz aufweisen, die niedriger ist als die Bitrate der Daten an den Eingängen der abhängigen Treiber (DS1,...DSn), jedoch eine gleiche Flankensteilheit haben.

3. Automatisches System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Taktsignale eine Frequenz aufweisen, die etwa ein Viertel der Bitrate der Daten an den Eingängen der abhängigen Treiber (DS1,...DSn) ist.

4. Automatisches System nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß die Ausgangsspannung des Komparators (CO) für die gesamte Periode des zweiten Taktsignals konstant ist und der Vergleich stattfindet, nachdem ihre Ausgangssignale (7, 8) zum hohen logischen Pegel wechseln.

Revendications

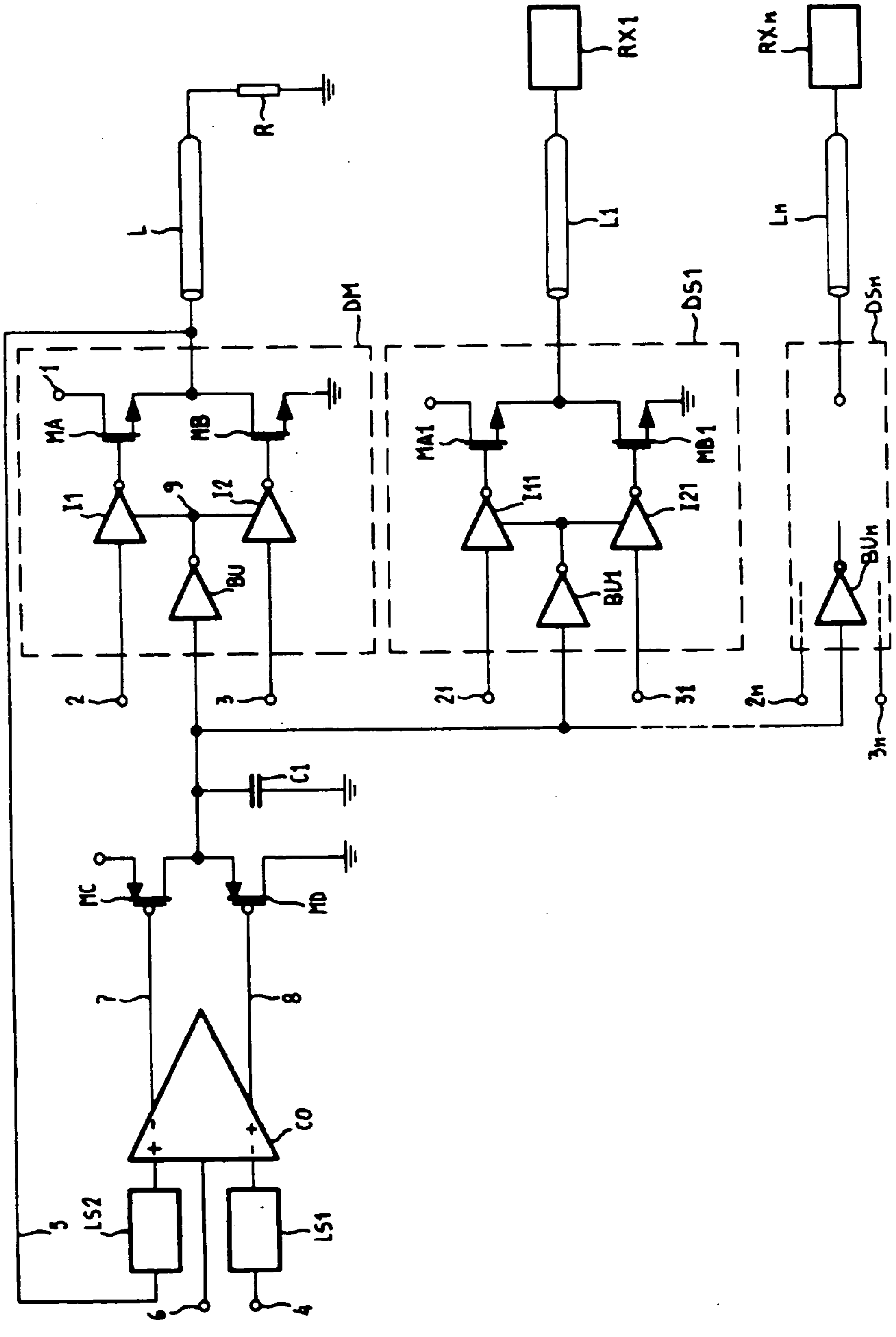
1. Système automatique pour l'adaptation de l'impédance de sortie des circuits de pilotage rapides en technologie CMOS, où l'impédance de sortie d'une pluralité de circuits de pilotage asservis (DS1..DSn) est contrôlée par un circuit pour la mesure et la correction de la désadaptation entre un des circuits de pilotage (DM), pris comme étalon et dédié à ce but, et l'impédance à l'entrée d'une ligne de transmission étalon (L), égale aux lignes (L1..Ln) connectées aux autres circuits de pilotage, la correction de l'impédance de sortie du circuit de pilotage étalon (DM) étant effectuée par un comparateur (CO) qui compare le voltage maximum d'un signal d'horloge fourni par ce circuit de pilotage étalon (DM) à l'entrée de la ligne étalon (L) avec un voltage de référence égal à moitié le voltage d'alimentation des étages de sortie des circuits de pilotage et sur la base du résultat de la comparaison ledit comparateur (CO) fournit un courant qui charge ou décharge périodiquement un condensateur (C1), de sorte à obtenir à ses terminaisons un voltage de contrôle de l'impédance des circuits de pilotage, caracté-

risé en ce que à l'entrée (2, 3) dudit circuit de pilotage étalon (DM) on envoye un premier signal d'horloge en produisant un signal périodique sur ladite ligne étalon (L) terminée par une résistance (R) égale à son impédance caractéristique et ledit signal périodique présent à l'entrée de la ligne étalon est comparé avec ledit voltage de référence dans ledit comparateur (CO) en correspondence des transitions d'un second signal d'horloge (sur 6) de fréquence égale à celle du premier signal d'horloge, mais en quadrature de manière à effectuer la comparaison au centre de la semi-période dans laquelle le voltage à l'entrée de la ligne étalon (L) est maximal, le résultat de la comparaison étant employé pour charger ou décharger un condensateur (C1), dont le voltage est appliqué à l'entrée d'une pluralité d'amplificateurs tampons, dont un (BU) contrôle l'impédance de sortie du circuit de pilotage étalon (DM) tandis que les autres (BU1...BUn) contrôlent les impédances de sortie des circuits de pilotage asservis (DS1...DSn).

2. Système automatique selon la revendication 1, caractérisé en ce que lesdits signaux d'horloge présentent une fréquence inférieure au débit des données aux entrées des circuits de pilotage asservis (DS1..DSn), mais une rapidité des fronts égale.

3. Système automatique selon les revendications 1 ou 2, caractérisé en ce que lesdits signaux d'horloge présentent une fréquence égale à environ un quart du débit des données aux entrées des circuits de pilotage asservis (DS1..DSn).

4. Système automatique selon l'une quelconque des revendications 1 à 3, caractérisé en ce que le voltage à la sortie dudit comparateur (CO) est constant pour toute la période du second signal d'horloge et que la comparaison a lieu après que ses sorties (7,8) ont atteint le niveau logique élevé.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Applic. #

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